Refine Search

Search Results -

Terms	Documents
(709/208 |709/224 |709/253 |340/3.1 |361/683 |710/15 |710/19 |710/100 |710/11 |710/300 |710/105 |710/107 |710/305 |710/315 |702/122 |370/464 |712/31 |714/47).ccls.	9158

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Search: L2

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, July 22, 2004 Printable Copy Create Case

Set Name	Query
side by side	
	DB=USPT,USOC; PLUR=YES; OP=OR
L2	710/15,19,100,11,300,105,107,305,315;702/122;340/3.1;709/208,224,253;712/31;370/464;714/4
	DB=DWPI; PLUR=YES; OP=OR
L1	710/15,19,100,11,300,105,107,305,315;702/122;340/3.1;709/208,224,253;712/31;370/464;714/4

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L2 and L3	101

Database:
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- US Patents Full-Text Database
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- IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text | Clear | Interrupt

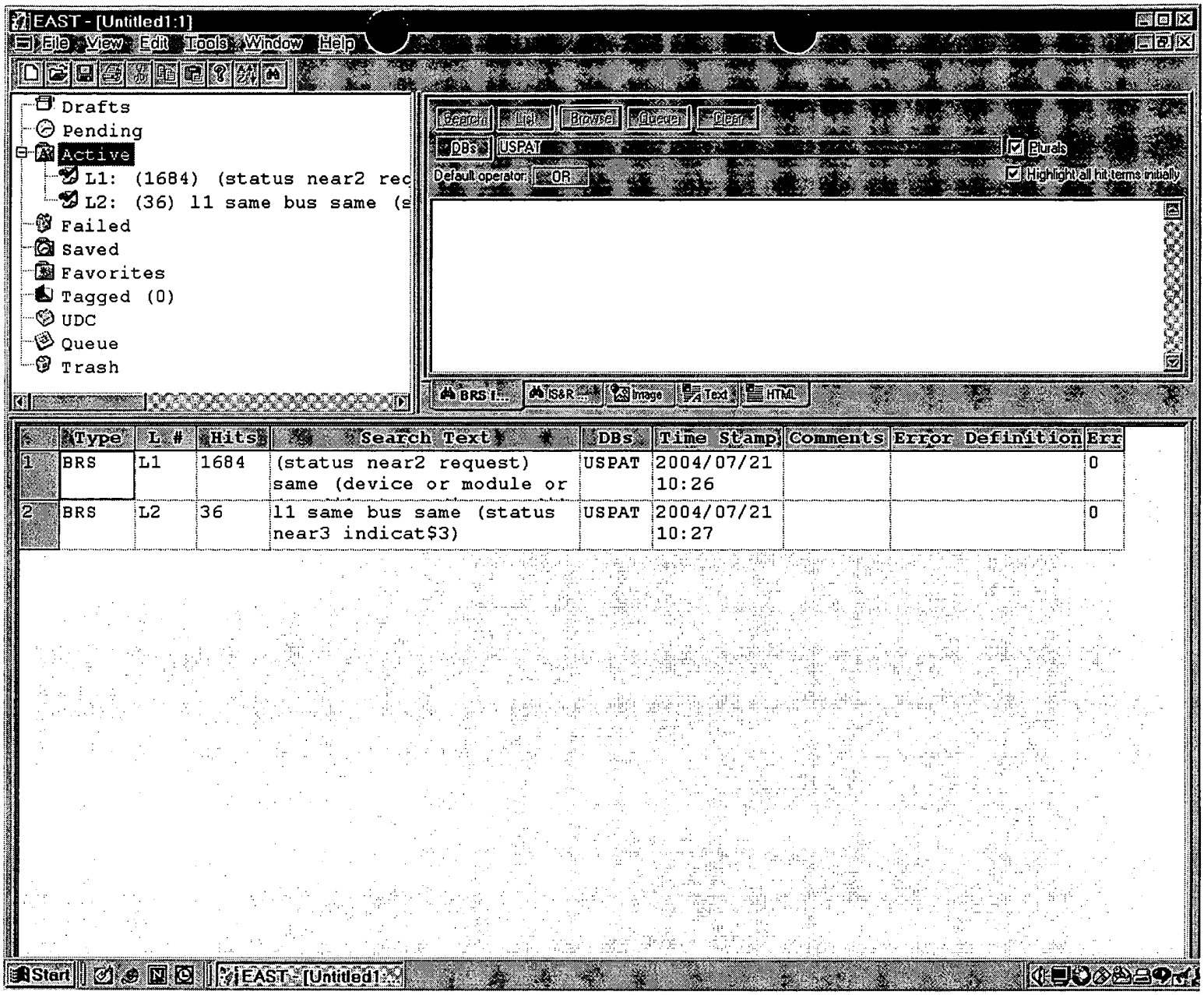
Search History

DATE: Thursday, July 22, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L4	l2 and L3
L3	(status near5 request) same (device or module or (I adj1 O) or (input adj1 output) or peripheral) sa
L2	710/15,19,100,11,300,105,107,305,315;702/122;340/3.1;709/208,224,253;712/31;370/464;714/4
	DB=DWPI; PLUR=YES; OP=OR
L1	710/15,19,100,11,300,105,107,305,315;702/122;340/3.1;709/208,224,253;712/31;370/464;714/4

END OF SEARCH HISTORY

h e b b cg b e e ch



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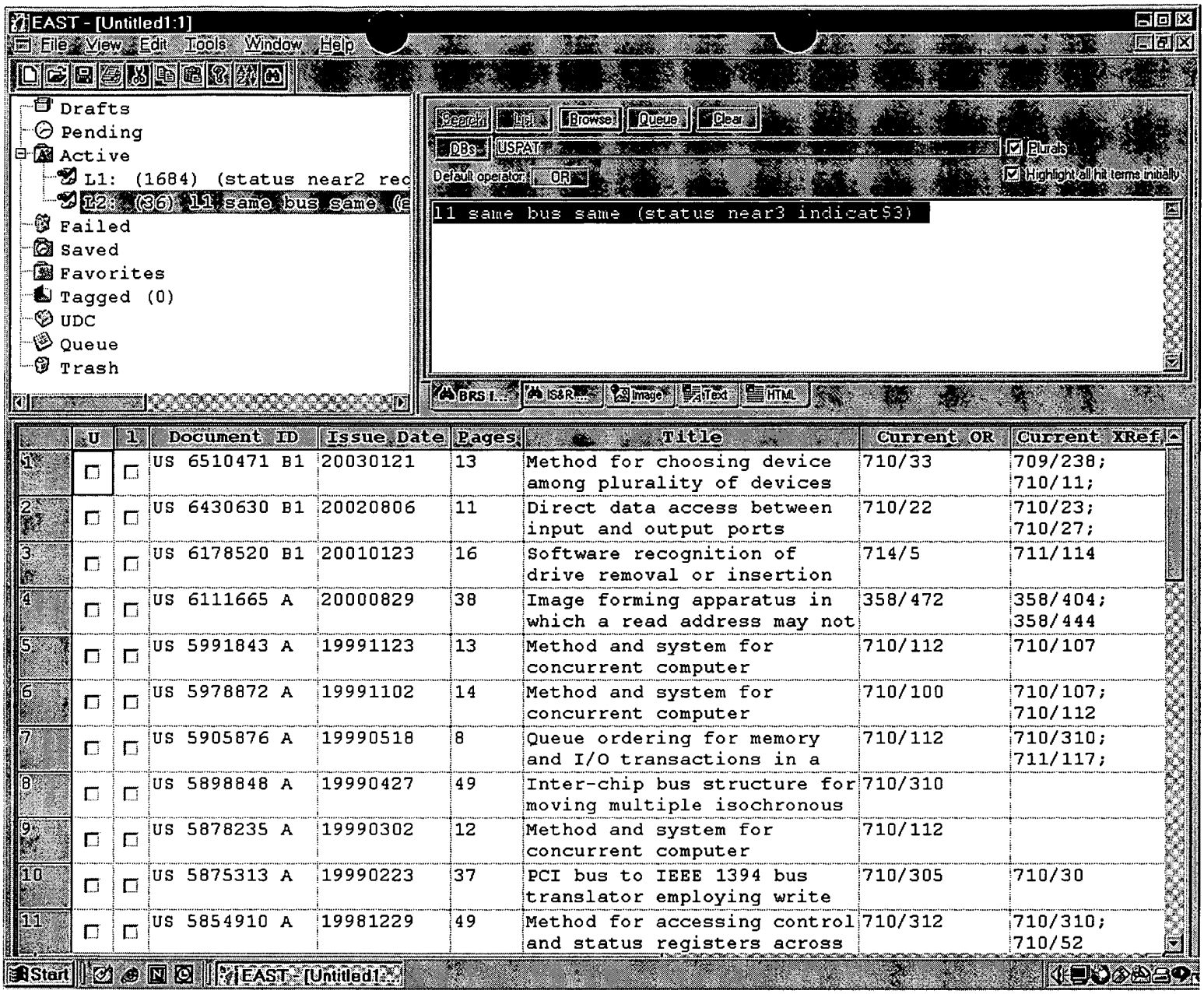
1	BRS	L1	1684	(status near2 request) same (device or module or	USPAT	2004/07/21 10:26			0
2	BRS	L2	36	l1 same bus same (status near3 indicat$3)	USPAT	2004/07/21 10:27			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6510471 B1	20030121	13	Method for choosing device among plurality of devices	710/33	709/238; 710/11;
2	☐	☐	US 6430630 B1	20020806	11	Direct data access between input and output ports	710/22	710/23; 710/27;
3	☐	☐	US 6178520 B1	20010123	16	Software recognition of drive removal or insertion	714/5	711/114
4	☐	☐	US 6111665 A	20000829	38	Image forming apparatus in which a read address may not	358/472	358/404; 358/444
5	☐	☐	US 5991843 A	19991123	13	Method and system for concurrent computer	710/112	710/107
6	☐	☐	US 5978872 A	19991102	14	Method and system for concurrent computer	710/100	710/107; 710/112
7	☐	☐	US 5905876 A	19990518	8	Queue ordering for memory and I/O transactions in a	710/112	710/310; 711/117;
8	☐	☐	US 5898848 A	19990427	49	Inter-chip bus structure for moving multiple isochronous	710/310	
9	☐	☐	US 5878235 A	19990302	12	Method and system for concurrent computer	710/112	
10	☐	☐	US 5875313 A	19990223	37	PCI bus to IEEE 1394 bus translator employing write	710/305	710/30
11	☐	☐	US 5854910 A	19981229	49	Method for accessing control and status registers across	710/312	710/310; 710/52

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status and request and indicat* Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **Efficient transmission of ARQ feedback for EGPRS radio link control**
Balachandran, K.; Ejzak, R.P.; Nanda, S.;
Vehicular Technology Conference, 1999. VTC 1999 - Fall. IEEE VTS 50th , Vol 3 , 19-22 Sept. 1999
Pages:1663 - 1669 vol.3

[Abstract] [PDF Full-Text (608 KB)] **IEEE CNF**

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Efficient transmission of ARQ feedback for EGPRS radio link control

Balachandran, K. Ejzak, R.P. Nanda, S.
Bell Labs., Lucent Technol., Holmdel, NJ, USA;

This paper appears in: **Vehicular Technology Conference, 1999. VTC 1999 - Fall. IEEE VTS 50th**

Meeting Date: 09/19/1999 - 09/22/1999
Publication Date: 19-22 Sept. 1999
Location: Amsterdam Netherlands
On page(s): 1663 - 1669 vol.3
Volume: 3
Reference Cited: 5
Number of Pages: 5 vol. (lxix+3056)
Inspec Accession Number: 6520852

Abstract:
ARQ feedback in enhanced general packet radio service (EGPRS) is provided through the use of bitmaps that **indicate** the receipt **status** of individual radio link control (RLC) blocks. The use of a robust coding and modulation scheme for the transmission of ARQ feedback limits the length of the bitmap that can be accommodated in a single feedback message to a fraction of the receiver window. Depending on the feedback frequency,

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round trip delay and the rate of transmission of RLC blocks, incomplete feedback may cause considerable protocol stalling. In this paper, the loss of throughput due to partial feedback is characterized. We also propose various techniques that minimize protocol stalling through the efficient transmission of multiple non-overlapping bitmaps that cover the receiver window. Simulation results show the relative benefits of the proposed techniques

Index Terms:

automatic repeat **request** feedback minimum shift keying packet radio networks protocols radio links telecommunication control ARQ feedback transmission EGPRS radio link control GMSK RLC blocks enhanced general packet radio service feedback frequency modulation scheme multiple non-overlapping bitmaps partial feedback protocol stalling minimization receiver window robust coding round trip delay simulation results transmission rate

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L3: Entry 4 of 10 File: USPT Oct 10, 1995

DOCUMENT-IDENTIFIER: US 5457787 A
TITLE: Interface circuit for controlling data transfers

Detailed Description Text (18):
The host 12 in the pre-read mode reads status register 50 in interface circuit 14 in response to the interrupt request IRQ from HDD 10 to know the status of HDD 10 before starting data transfer. To this end, host 12 transmits signals indicating read of status register 50, that is, an address of status register 50 and an input/output read signal -IOR over bus 16A. In response to the signals, register selector 40 generates a signal S5 for selecting status register 50 to cause its contents to be gated to bus 16B. Status register 50 contains not only the DRQ bit described above, but also a plurality of status bits representing the status of HDD 10 such as a busy bit indicating that HDD 10 is busy, an error bit indicating that an error has occurred during the command execution, etc.

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

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L3: Entry 4 of 10 File: USPT Oct 10, 1995

US-PAT-NO: 5457787
DOCUMENT-IDENTIFIER: US 5457787 A

TITLE: Interface circuit for controlling data transfers

DATE-ISSUED: October 10, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Asano; Hideo	Machida			JP
Murakami; Masayuki	Fujisawa			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 08/ 130951 [PALM]
DATE FILED: October 4, 1993

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	4-264371	October 2, 1992

INT-CL: [06] G06 F 13/14

US-CL-ISSUED: 395/375; 364/DIG.1, 364/DIG.2, 364/236.2, 364/241.2, 364/248.1, 364/260, 364/941, 364/941.1
US-CL-CURRENT: 710/305

FIELD-OF-SEARCH: 395/275, 395/500, 395/200, 395/700, 395/800, 395/375, 364/DIG.1MSFile, 364/DIG.2MSFile

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4509113	April 1985	Heath	395/275
☐	4607328	August 1986	Furukawa et al.	395/250
☐	4947366	August 1990	Johnson	395/275

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☐	5014237	May 1991	Masters et al.	395/500

ART-UNIT: 235

PRIMARY-EXAMINER: Harrell; Robert B.

ATTY-AGENT-FIRM: Gamon; Owen J.

ABSTRACT:

An interface circuit for a peripheral device is disclosed that can accurately cope with any host with the same hardware whether the host is in the pre-read mode or the post-read mode and can send an interrupt request to the host practically without a waiting time if the host is in the post-read mode. The interface circuit generates an interrupt request (IRQ) to a host in response to a data request (DRQ) from a peripheral device (HDD) and drops the interrupt request if the status of the peripheral device is read by the host; it detects that the host operates in a post-read mode, and responds to the post-read mode detect signal and the status reading by the host in order to enable the regeneration of the interrupt request to the host.

24 Claims, 6 Drawing figures

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L6: Entry 1 of 8 File: USPT Oct 28, 2003

DOCUMENT-IDENTIFIER: US 6640312 B1

**** See image for Certificate of Correction ****

TITLE: System and method for handling device retry requests on a communication medium

Abstract Text (1):

A system and method for transferring data over a communications medium. A host is coupled to a device through a serial bus lacking error handling capabilities, such as an IEEE 1394 bus. The host may control the device by sending requests accessing its memory registers. The host generates a first request to the device to access a memory address location of the device, and which includes an address and status information indicating whether a prior request to the memory address location returned successfully. The device examines the status information to determine if it is a retry of a prior request, and if so, determines if the prior request completed successfully to the memory address location by comparing the address and data transfer size of the first request to those of the prior request. If identical, then the prior request completed successfully to the memory address location, and the request is ignored. Otherwise, the device retries the prior request. If the first request is not a retry the device performs it and returns an acknowledgement to the host indicating successful completion. If the host does not receive valid acknowledgement, it retries the first request, otherwise, it completes a transaction associated with the first request. Then, a new transaction request may be received which results in a new request being generated by the host to access the memory address location. The host may manipulate the status information in the new request to indicate that the first request to the memory address location returned successfully.

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L6: Entry 1 of 8 File: USPT Oct 28, 2003

US-PAT-NO: 6640312
DOCUMENT-IDENTIFIER: US 6640312 B1
**** See image for Certificate of Correction ****

TITLE: System and method for handling device retry requests on a communication medium

DATE-ISSUED: October 28, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Thomson; Andrew	Austin	TX		
Madden; David W.	Austin	TX		
Sescila; Glen	Pflugerville	TX		
Vrancic; Aljosa	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
National Instruments Corporation	Austin	TX			02

APPL-NO: 09/ 629349 [PALM]
DATE FILED: August 1, 2000

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/5; 714/9, 714/43
US-CL-CURRENT: 714/5; 714/43, 714/9

FIELD-OF-SEARCH: 714/4, 714/5, 714/9, 714/43, 714/44

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5875313	February 1999	Sescila, III et al.	
☐	5923673	July 1999	Henrikson	371/20.1
☐	5937175	August 1999	Sescila, III et al.	
☐	5953511	September 1999	Sescila, III et al.	
☐	6389560	May 2002	Chew	714/43

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☐	2001/0044914	November 2001	Nakano et al.	714/43
☐	2002/0049933	April 2002	Nyu	714/43

ART-UNIT: 2184

PRIMARY-EXAMINER: Baderman; Scott

ASSISTANT-EXAMINER: Bonura; Timothy M

ATTY-AGENT-FIRM: Meyertons Hood Kivlin Kowert & Goetzel, P.C. Hood; Jeffrey C.

ABSTRACT:

A system and method for transferring data over a communications medium. A host is coupled to a device through a serial bus lacking error handling capabilities, such as an IEEE 1394 bus. The host may control the device by sending requests accessing its memory registers. The host generates a first request to the device to access a memory address location of the device, and which includes an address and status information indicating whether a prior request to the memory address location returned successfully. The device examines the status information to determine if it is a retry of a prior request, and if so, determines if the prior request completed successfully to the memory address location by comparing the address and data transfer size of the first request to those of the prior request. If identical, then the prior request completed successfully to the memory address location, and the request is ignored. Otherwise, the device retries the prior request. If the first request is not a retry the device performs it and returns an acknowledgement to the host indicating successful completion. If the host does not receive valid acknowledgement, it retries the first request, otherwise, it completes a transaction associated with the first request. Then, a new transaction request may be received which results in a new request being generated by the host to access the memory address location. The host may manipulate the status information in the new request to indicate that the first request to the memory address location returned successfully.

24 Claims, 8 Drawing figures

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L9: Entry 21 of 22 File: USPT Jan 22, 1985

DOCUMENT-IDENTIFIER: US 4495564 A
TITLE: Multi sub-channel adapter with single status/address register

Abstract Text (1):
An improved adapter for a programmed control unit arranged to be operated in facilitating I/O operations between one or more I/O devices and a CPU through a channel. The improved adapter includes a local store which store has a hardware register dedicated to store device status and the associated address in connection with test I/O commands. Thus, in accordance with the method of the invention on receiving a status request the improved adapter responds immediately with a response indicating that the information is not immediately available, for example, a busy response. The improved adapter initiates an interrupt to the program control unit to obtain the requested status information, which is then stored in dedicated hardware registers of the local store. On the next subsequent test I/O command to the same address, the improved adapter responds with the status as read from the dedicated hardware register. In another aspect the invention provides an improved adapter which includes communication path means, for example hardware registers, passing data to and from the channel and attached devices, and a further hardware register of sufficient capacity to store a status word and an associated address. The adapter also includes a bus for transferring a status word and associated address from the attached control unit in response to a channel received command to the further hardware register and, control circuitry which is responsive to a subsequent status request and command associated with the associated address, for placing the status word from the further hardware register on the channel. The adapter supports both host or control unit initiated I/O status transfers, i.e. both synchronous and asynchronous.

Previous Doc Next Doc Go to Doc#

L9: Entry 21 of 22 File: USPT Jan 22, 1985

US-PAT-NO: 4495564
DOCUMENT-IDENTIFIER: US 4495564 A

TITLE: Multi sub-channel adapter with single status/address register

DATE-ISSUED: January 22, 1985

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Draper; Wilburn D.	Raleigh	NC		
Laakso; Melvin T.	Cary	NC		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 06/ 291741 [PALM]
DATE FILED: August 10, 1981

INT-CL: [03] G06F 3/04

US-CL-ISSUED: 364/200
US-CL-CURRENT: 710/17

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3311889	March 1967	Birmingham et al.	
☐	3596256	June 1971	Alpert et al.	340/172.5
☐	3673576	June 1972	Donaldson, Jr.	340/172.5
☐	3680054	July 1972	Bunker et al.	364/200
☐	3725864	April 1973	Clark et al.	364/200
☐	3833888	September 1974	Stafford et al.	340/172.5
☐	3902162	August 1975	Parkinson et al.	340/172.5

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☐	3934232	January 1976	Curley et al.	340/172.5
☐	3997896	December 1976	Cassarino et al.	364/200
☐	4003033	January 1977	O'Keefe et al.	340/172.5
☐	4126897	November 1978	Capowski et al.	364/200
☐	4128883	December 1978	Duke et al.	364/200
☐	4170038	October 1979	Bouvier	364/200
☐	4245300	January 1981	Kaufman et al.	364/200
☐	4246637	January 1981	Brown et al.	364/200

OTHER PUBLICATIONS

Microsystems, Inc., Micro 812 Communications Processor, Apr. 1970, pp. 1-14.
Steele & Mattson, Computer Design, Architecture of a Universal Communications Processor, Nov. 1973, pp. 63-68.

ART-UNIT: 237

PRIMARY-EXAMINER: Chan; Eddie P.

ATTY-AGENT-FIRM: Frisone; John B.

ABSTRACT:

An improved adapter for a programmed control unit arranged to be operated in facilitating I/O operations between one or more I/O devices and a CPU through a channel. The improved adapter includes a local store which store has a hardware register dedicated to store device status and the associated address in connection with test I/O commands. Thus, in accordance with the method of the invention on receiving a status request the improved adapter responds immediately with a response indicating that the information is not immediately available, for example, a busy response. The improved adapter initiates an interrupt to the program control unit to obtain the requested status information, which is then stored in dedicated hardware registers of the local store. On the next subsequent test I/O command to the same address, the improved adapter responds with the status as read from the dedicated hardware register. In another aspect the invention provides an improved adapter which includes communication path means, for example hardware registers, passing data to and from the channel and attached devices, and a further hardware register of sufficient capacity to store a status word and an associated address. The adapter also includes a bus for transferring a status word and associated address from the attached control unit in response to a channel received command to the further hardware register and, control circuitry which is responsive to a subsequent status request and command associated with the associated address, for placing the status word from the further hardware register on the channel. The adapter supports both host or control unit initiated I/O status transfers, i.e. both synchronous and asynchronous.

10 Claims, 5 Drawing figures

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US-PAT-NO: 5797037

DOCUMENT-IDENTIFIER: US 5797037 A

TITLE: Interrupt request control logic reducing the number of interrupts required for I/O data transfer

---------- KWIC ---------

Detailed Description Text - DETX (3):

When the first byte of the data has been transferred from a data source 8 (for example, data channel or storage) to the I/O controller 4, the latter asserts a DMA request signal that is received by the DMA controller 2. In some applications, separate DMA channels are provided for transferring status information and input data. In particular, input data may be accompanied with a data descriptor that indicates the status of the data related events. For example, such a descriptor may be used to report parity and/or system errors. Also, it may describe what to do with the accompanied data or request a specific procedure to be used for handling the accompanied data. In this case, as shown in FIG. 1, the DMA controller 2 is supplied with separate DMA requests for transferring status information (STATUS DMA REQ) and for transferring input data (INP DMA REQ). In response to any one of the DMA requests, the DMA controller 2 asserts a hold request signal (HOLD) to seize address, data and control buses from a central processing unit (CPU) 10. When the CPU 10 completes the current cycle, it asserts HLDA to inform the DMA controller 2 that its request is granted. The DMA controller 2 responds by sending DMA acknowledge for status information and input data (STATUS DMA ACK and INP DMA ACK, respectively) to the I/O controller 4. The I/O controller gates the status information and input data to a data bus 12 to the DRAM memory 6 and drops the DMA requests.

US005797037A

United States Patent [19]

Ecclesine

[11] **Patent Number: 5,797,037**

[45] **Date of Patent: Aug. 18, 1998**

[54] **INTERRUPT REQUEST CONTROL LOGIC REDUCING THE NUMBER OF INTERRUPTS REQUIRED FOR I/O DATA TRANSFER**

[75] Inventor: **Peter Ecclesine**, Livermore, Calif.

[73] Assignee: **Cirrus Logic, Inc.**, Fremont, Calif.

[21] Appl. No.: 414,474

[22] Filed: Mar. 31, 1995

[51] Int. Cl.[6] G06F 13/14; G06F 9/46

[52] U.S. Cl. 395/868; 395/848; 395/739

[58] Field of Search 395/868, 842, 395/848, 733, 739, 735

[56] **References Cited**

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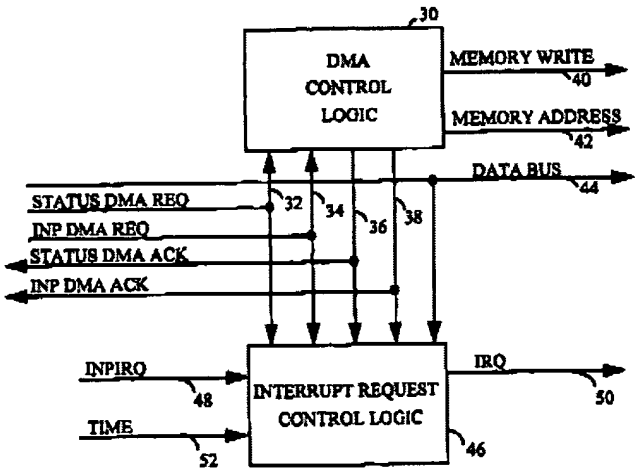
5,291,608	3/1994	Flory	395/725
5,367,688	11/1994	Mayer et al.	395/725
5,459,870	10/1995	Iwata et al.	395/734
5,484,726	1/1996	Kimuki et al.	395/200.01
5,530,874	6/1996	Emery et al.	395/735

Primary Examiner—Thomas C. Lee
Assistant Examiner—Rehana Perveen
Attorney, Agent, or Firm—Lowe, Price LeBlanc & Becker; Frank D. Nguyen

[57] **ABSTRACT**

A DMA data transfer system is provided with an interrupt request controller that has pass through logic, data limit logic, stale data logic and error detecting logic to monitor for predetermined conditions. A request for an interrupt sent to a central processor is generated by the interrupt request controller when an input interrupt request is applied to the interrupt request controller and one of the following conditions is met: 1) no previous DMA requests had occurred for a predetermined time interval; 2) a preset limit for the amount of data being transferred is reached; 3) no new requests for DMA transfer occur for preset time intervals; or 4) the status indicates an error in the data being transferred. or priority handling of the data is requested. By making sure one of the predetermined conditions is met before generating an interrupt request, the number of interrupt requests to the central processing unit is greatly reduced and the throughput of the system is increased.

22 Claims, 8 Drawing Sheets



US-PAT-NO: 4839794

DOCUMENT-IDENTIFIER: US 4839794 A

TITLE: Pseudo-status signal generator

---------- KWIC ---------

Brief Summary Text - BSTX (4):

FIG. 1 is a block diagram showing an example of a conventional prior art arrangement of an electronic data transfer apparatus. In FIG. 1, numeral 1 denotes a main device, such as a CRT device, and numeral 2 denotes an input/output requesting device, such as an input/output controller. The main device 1 and the input/output requesting device are connected to each other through a data bus 3. The data bus 3 includes an input request signal line 3A for transmitting a data input request from the input/output requesting device 2 to the main device, an output request signal line 3B for transmitting a data output request, a status request signal line 3C for requesting status information, such as "busy" or "ready", from the main device 1, and data signal lines 3D for transmitting data between the two devices. The main device 1 may also contain a status signal generator (not shown) for indicating the actual status information to an external device.

United States Patent [19]
Okura

[11] **Patent Number: 4,839,794**
[45] **Date of Patent: Jun. 13, 1989**

[54] **PSEUDO-STATUS SIGNAL GENERATOR**

[75] Inventor: Makoto Okura, Kamakura, Japan
[73] Assignee: Mitsubishi Denki Kabushiki Kaisha, Japan

[21] Appl. No.: 122,151
[22] Filed: Nov. 18, 1987

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 80,393, May 18, 1987, abandoned.

[30] Foreign Application Priority Data

May 20, 1986 [JP] Japan 61-113641

[51] Int. Cl.[4] G06F 13/14
[52] U.S. Cl. 364/200
[58] Field of Search ... 364/200 MS File, 900 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

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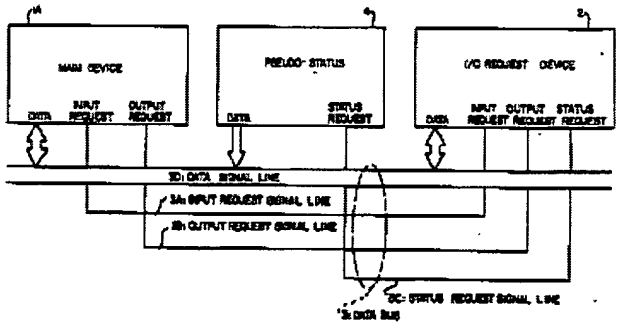
4,493,574 1/1985 Hofacker 364/200
4,534,417 6/1985 Kimoto 364/200
4,688,770 10/1987 Ratna et al. 364/900
4,723,325 2/1988 Fukuda et al. 364/200

Primary Examiner—David L. Clark
Attorney, Agent, or Firm—Leydig, Voit & Mayer

[57] **ABSTRACT**

An electronic data transfer apparatus comprises a main device connected to input and output data, an input-/output requesting device connected to the main device for controlling data input and output operations, a data bus provided between the main device and the input-/output requesting device to facilitate connection therebetween for transferring data, and a pseudo-status signal generator interposed between the main device and the input/output requesting device for alternately generating status signals representing ready and busy states of the main device in accordance with a status request from the input/output requesting device whereby data transfer speed therebetween is substantially improved.

3 Claims, 6 Drawing Sheets



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L9: Entry 9 of 21 File: USPT Sep 29, 1998

DOCUMENT-IDENTIFIER: US 5815082 A
TITLE: Local communication bus system and apparatuses for use in such a system

Brief Summary Text (2):
The invention relates to a local communication bus system comprising a serial control bus connecting a plurality of apparatuses addressable via the bus as devices, each device including at least one functional element addressable via the bus as a subdevice, the subdevices in the system including a control subdevice and a further subdevice, the control subdevice including means for generating a subdevice status request message addressed to the further subdevice in the system, while the further subdevice includes means responsive to the subdevice status request message for returning a subdevice status message to the control subdevice.

CLAIMS:

1. A local communication bus system comprising a serial control bus coupled to a plurality of devices, each device comprising a control subdevice and a further subdevice, each device, control subdevice and further subdevice being addressable using said serial control bus, wherein said control subdevice comprises means for generating a first status request message addressed to said further subdevice, and wherein said further subdevice comprises:

a) means responsive to said first status request message for generating a first further subdevice status message to said control subdevice; and

b) means responsive to a change in status in said further subdevice for generating an updated further subdevice status message to said control subdevice without receiving an additional status request message from said control subdevice, if and only if said further subdevice has previously received said first status request message.

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L9: Entry 9 of 21 File: USPT Sep 29, 1998

US-PAT-NO: 5815082
DOCUMENT-IDENTIFIER: US 5815082 A

TITLE: Local communication bus system and apparatuses for use in such a system

DATE-ISSUED: September 29, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Welmer; Harm J.	Sutton			GB2

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
DB2 Systems Company Limited	Surrey RH1 1DL			GB2	03

APPL-NO: 07/ 853373 [PALM]
DATE FILED: March 18, 1992

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
GB	9106113.5	March 22, 1991
GB	9113793.5	June 26, 1991

INT-CL: [06] H04 Q 1/00

US-CL-ISSUED: 340/825.07; 370/451
US-CL-CURRENT: 340/3.51; 340/825.24, 370/451

FIELD-OF-SEARCH: 340/825.07, 340/825.63, 340/825.5, 340/825.51, 340/825.08, 340/504, 340/505, 340/500, 340/825.52, 340/870.03, 370/85.1, 370/85.8, 370/241, 370/245, 370/247, 370/251, 370/252, 370/257, 370/364, 370/450, 370/449, 370/451

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4716408	December 1987	O'Connor et al.	340/825.07
☐	4939746	July 1990	Children	455/33.2
☐	4942571	July 1990	Moller et al.	370/85.1

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☐	5054022	October 1991	Van Steenbrugge	370/438
☐	5157658	October 1992	Arai et al.	340/825.07
☐	5189409	February 1993	Okuno	340/825.63
☐	5235619	August 1993	Beyers et al.	455/5.1

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0315158	May 1989	EP	
0369382	May 1990	EP	
2223114	March 1990	GB	

OTHER PUBLICATIONS

"Targetted MCU Design For Control Networks", by S. Heath, Electronic Product Design, vol. 12, No. 7, Jul. 1991.

ART-UNIT: 272

PRIMARY-EXAMINER: Ton; Dang

ATTY-AGENT-FIRM: Wieghaus; Brian J.

ABSTRACT:

A number of domestic audio/video apparatuses (10-14) are connected to a serial control bus (D2B, 16). Each apparatus is addressable via the bus as a device and contains functional elements addressable on subdevices. One apparatus (14) includes an on-screen display subdevice (41) and a first control subdevice (24). Subdevice status messages are defined whereby a control subdevice can ask to be informed of the status of a further subdevice (e.g. 26), and in particular to be informed automatically of any change in status without the need for continuous polling of subdevices. The subdevice status messages can be used to obtain early confirmation of a signal path being established through the system.

29 Claims, 3 Drawing figures

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L9: Entry 9 of 21 File: USPT Sep 29, 1998

US-PAT-NO: 5815082
DOCUMENT-IDENTIFIER: US 5815082 A

TITLE: Local communication bus system and apparatuses for use in such a system

DATE-ISSUED: September 29, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Welmer; Harm J.	Sutton			GB2

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
DB2 Systems Company Limited	Surrey RH1 1DL			GB2	03

APPL-NO: 07/ 853373 [PALM]
DATE FILED: March 18, 1992

FOREIGN-APPL-PRIORITY-DATA:

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GB	9106113.5	March 22, 1991
GB	9113793.5	June 26, 1991

INT-CL: [06] H04 Q 1/00

US-CL-ISSUED: 340/825.07; 370/451
US-CL-CURRENT: 340/3.51; 340/825.24, 370/451

FIELD-OF-SEARCH: 340/825.07, 340/825.63, 340/825.5, 340/825.51, 340/825.08, 340/504, 340/505, 340/500, 340/825.52, 340/870.03, 370/85.1, 370/85.8, 370/241, 370/245, 370/247, 370/251, 370/252, 370/257, 370/364, 370/450, 370/449, 370/451

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4716408	December 1987	O'Connor et al.	340/825.07
☐	4939746	July 1990	Children	455/33.2
☐	4942571	July 1990	Moller et al.	370/85.1

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☐	5054022	October 1991	Van Steenbrugge	370/438
☐	5157658	October 1992	Arai et al.	340/825.07
☐	5189409	February 1993	Okuno	340/825.63
☐	5235619	August 1993	Beyers et al.	455/5.1

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0315158	May 1989	EP	
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2223114	March 1990	GB	

OTHER PUBLICATIONS

"Targetted MCU Design For Control Networks", by S. Heath, Electronic Product Design, vol. 12, No. 7, Jul. 1991.

ART-UNIT: 272

PRIMARY-EXAMINER: Ton; Dang

ATTY-AGENT-FIRM: Wieghaus; Brian J.

ABSTRACT:

A number of domestic audio/video apparatuses (10-14) are connected to a serial control bus (D2B, 16). Each apparatus is addressable via the bus as a device and contains functional elements addressable on subdevices. One apparatus (14) includes an on-screen display subdevice (41) and a first control subdevice (24). Subdevice status messages are defined whereby a control subdevice can ask to be informed of the status of a further subdevice (e.g. 26), and in particular to be informed automatically of any change in status without the need for continuous polling of subdevices. The subdevice status messages can be used to obtain early confirmation of a signal path being established through the system.

29 Claims, 3 Drawing figures

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L9: Entry 12 of 21 File: USPT Aug 8, 1989

DOCUMENT-IDENTIFIER: US 4855730 A
TITLE: Component audio/video system with timed control of plural peripheral devices

Brief Summary Text (8):
It has been recognized that a large number of audio/video and audio-only devices may be combined in a unified home entertainment system by providing a central control unit coupled via a digital data bus to individual device of the system. An example of such a system is described in B. W. Beyers, Jr. in U.S. Pat. No. 4,581,645 entitled DISTRIBUTED SWITCHED COMPONENT AUDIO/VIDEO SYSTEM. Other examples include U.S. Pat. No. 4,337,480 of Bourassin et al. entitled DYNAMIC AUDIO-VIDEO INTERCONNECTION SYSTEM and U.S. Pat. No. 4,488,179 of Kruger et al. entitled TELEVISION VIEWING CENTER SYSTEM. R. A. Pitsch describes a bus-oriented system in an article entitled "Dimensia: The Next Dimension of Sight and Sound" published in RCA Engineer, July/August edition, 1985, at pp. 66-70. In the described system the control bus provides two-way communication between a central controller and a plurality of individual device controllers. By this feature a user may transmit a status request and receive a response (displayed on the screen of his TV receiver) that gives the status (e.g., play, pause, etc.) of any selected device in his system. The user may also transmit commands via the two-way data bus to select and control the "status" or operating mode of individual audio and video peripheral devices connected to the bus.

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L9: Entry 12 of 21 File: USPT Aug 8, 1989

US-PAT-NO: 4855730
DOCUMENT-IDENTIFIER: US 4855730 A

TITLE: Component audio/video system with timed control of plural peripheral devices

DATE-ISSUED: August 8, 1989

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Venners; Howard W.	Indianapolis	IN		
Beyers Jr.; Billy W.	Greenfield	IN		
Hailey; James E.	Indianapolis	IN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
RCA Licensing Corporation	Princeton	NJ			02

APPL-NO: 07/ 048107 [PALM]
DATE FILED: May 8, 1987

INT-CL: [04] H04Q 9/00, G08C 23/00

US-CL-ISSUED: 340/825.24; 340/825.25, 358/194.1
US-CL-CURRENT: 340/825.24; 340/825.25, 348/734

FIELD-OF-SEARCH: 340/825.06, 340/825.07, 340/825.22, 340/825.24, 340/825.25, 455/4, 455/5, 455/353, 358/181, 358/188, 358/194.1, 358/189, 358/335, 360/74.1, 360/33.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3922641	November 1975	Gates Jr.	340/825.5
☐	4279012	July 1981	Beckedorff et al.	340/825.22
☐	4337480	June 1982	Bourassin et al.	358/93
☐	4400735	August 1983	Strammello Jr.	358/181
☐	4418333	November 1983	Schwarzbach et al.	340/825.22
☐	4488179	December 1984	Kruger et al.	358/181

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☐	4527204	July 1985	Kozakai et al.	360/33.1
☐	4581645	April 1986	Beyers Jr.	358/181
☐	4628370	December 1986	Fukuoka	360/15
☐	4631601	December 1986	Brugliera et al.	358/335
☐	4649428	March 1987	Jones et al.	358/194.1

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0129286	December 1984	EP	340/365VL

OTHER PUBLICATIONS

R. A. Pitsch, "Dimensia, The Next Dimension of Sight and Sound," RCA Engineer, Jul/Aug. 1985, pp. 66-70.

ART-UNIT: 264

PRIMARY-EXAMINER: Yusko; Donald J.

ASSISTANT-EXAMINER: Holloway III; Edwin C.

ATTY-AGENT-FIRM: Rasmussen; Paul J. Coalter; Richard G. Emanuel; Peter M.

ABSTRACT:

A component audio/video system includes a system controller having an input/output port adapted for connection via a bidirectional data bus to a plurality of peripheral audio/video devices. At times determined by a system master clock the controller transmits, via the bidirectional bus, user programmed sequences of commands at user specified times to user selected peripheral devices for controlling the operating modes thereof. After transmission of a command of a sequence, the controller monitors the bus to detect a received return status message from the selected device and in response to the received message selectively (1) re-transmits the last command, (2) interrupts the transmission and (3) transmits a further command in the sequence whereby a number of individual devices may be controlled by a single master clock and the possiblility of conflict between a currently transmitted command and a current device operating mode is minimized.

4 Claims, 2 Drawing figures

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L9: Entry 12 of 21 File: USPT Aug 8, 1989

US-PAT-NO: 4855730
DOCUMENT-IDENTIFIER: US 4855730 A

TITLE: Component audio/video system with timed control of plural peripheral devices

DATE-ISSUED: August 8, 1989

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Venners; Howard W.	Indianapolis	IN		
Beyers Jr.; Billy W.	Greenfield	IN		
Hailey; James E.	Indianapolis	IN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
RCA Licensing Corporation	Princeton	NJ			02

APPL-NO: 07/ 048107 [PALM]
DATE FILED: May 8, 1987

INT-CL: [04] H04Q 9/00, G08C 23/00

US-CL-ISSUED: 340/825.24; 340/825.25, 358/194.1
US-CL-CURRENT: 340/825.24; 340/825.25, 348/734

FIELD-OF-SEARCH: 340/825.06, 340/825.07, 340/825.22, 340/825.24, 340/825.25, 455/4, 455/5, 455/353, 358/181, 358/188, 358/194.1, 358/189, 358/335, 360/74.1, 360/33.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3922641	November 1975	Gates Jr.	340/825.5
☐	4279012	July 1981	Beckedorff et al.	340/825.22
☐	4337480	June 1982	Bourassin et al.	358/93
☐	4400735	August 1983	Strammello Jr.	358/181
☐	4418333	November 1983	Schwarzbach et al.	340/825.22
☐	4488179	December 1984	Kruger et al.	358/181

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☐	4527204	July 1985	Kozakai et al.	360/33.1
☐	4581645	April 1986	Beyers Jr.	358/181
☐	4628370	December 1986	Fukuoka	360/15
☐	4631601	December 1986	Brugliera et al.	358/335
☐	4649428	March 1987	Jones et al.	358/194.1

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0129286	December 1984	EP	340/365VL

OTHER PUBLICATIONS

R. A. Pitsch, "Dimensia, The Next Dimension of Sight and Sound," RCA Engineer, Jul/Aug. 1985, pp. 66-70.

ART-UNIT: 264

PRIMARY-EXAMINER: Yusko; Donald J.

ASSISTANT-EXAMINER: Holloway III; Edwin C.

ATTY-AGENT-FIRM: Rasmussen; Paul J. Coalter; Richard G. Emanuel; Peter M.

ABSTRACT:

A component audio/video system includes a system controller having an input/output port adapted for connection via a bidirectional data bus to a plurality of peripheral audio/video devices. At times determined by a system master clock the controller transmits, via the bidirectional bus, user programmed sequences of commands at user specified times to user selected peripheral devices for controlling the operating modes thereof. After transmission of a command of a sequence, the controller monitors the bus to detect a received return status message from the selected device and in response to the received message selectively (1) re-transmits the last command, (2) interrupts the transmission and (3) transmits a further command in the sequence whereby a number of individual devices may be controlled by a single master clock and the possiblility of conflict between a currently transmitted command and a current device operating mode is minimized.

4 Claims, 2 Drawing figures

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L1: Entry 8 of 201 File: USPT Jun 22, 2004

DOCUMENT-IDENTIFIER: US 6753928 B1
TITLE: Method and apparatus for providing feedback during programming of a television apparatus

Detailed Description Text (6):
The television receiver 12 shown in FIG. 1 also includes a main microprocessor (uP) 36 for controlling components of the television receiver such as tuners 32, 33, picture-in-picture processing unit 38 and video signal processor 40. As used herein, the term "microprocessor" represents various devices including, but not limited to, microprocessors, microcomputers, microcontrollers and controllers. Microprocessor (uP) 36 controls the system by sending and receiving both commands and data via serial data bus I2C_BUS that utilizes the well-known I.sup.2 C serial data bus protocol. More specifically, central processing unit (CPU) 42 within uP 36 executes control programs contained within memory, such as EEPROM 44 shown in FIG. 1, in response to commands provided by a user, e.g., via IR remote control 28 and IR receiver 46. For example, activation of a "CHANNEL UP" feature on the remote control 28 causes CPU 42 to send a "change channel" command along with channel data to tuner 32 via I2C_BUS serial data bus. Consequently, tuner 32 tunes the next channel in the channel scan list. Another example of a control program stored in EEPROM 44 is software for implementing the operations shown in FIG. 2, to be described in greater detail hereinafter.

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L1: Entry 41 of 201 File: USPT Nov 25, 2003

DOCUMENT-IDENTIFIER: US 6653863 B1
TITLE: Method and apparatus for improving bus capacity

Brief Summary Text (4):
The I2C bus was developed in the early 1980's to provide an easy way to connect a computer processor unit (CPU) to other peripheral semiconductor devices located in a television set.

Brief Summary Text (6):
Furthermore, a large number of control lines imply that a system is more susceptible to disturbances by Electromagnetic Compatibility (EMC) and Electrostatic Discharge (ESD). The research done by Philips Labs in Eindhoven (The Netherlands) resulted in a two-wire communication bus called the I2C bus. I2C is an acronym for Inter-IC bus. The I2C bus' name literally explains its purpose: to provide a communication link between integrated circuits.

Brief Summary Text (7):
Today, the extent of this I2C bus goes much further than audio and video equipment. The I2C bus is generally accepted in the electronics industry. Offspring of the I2C bus, such as D2B bus and ACCESS bus, have found their ways into computer peripherals like keyboards, mice, printers, monitors, etc. The I2C bus and similar arrangements have been adopted by several leading chip manufacturers such as Xicor, SGS-Thomson, Siemens, Intel, TI, Maxim, Atmel, and Analog Devices.

Brief Summary Text (8):
An I2C bus physically comprises two active bus signal lines, conductors or wires and a ground connection. Both of the active wires, having acronyms of SDA and SCL, are bidirectional, where SDA is the serial data line and SCL is the serial clock line. This means that these lines can be driven either by the semiconductor device or an external device. To avoid damage to the semiconductor device; i.e., commonly known as "the fried chip" effect, these bus signal lines typically use open-collector or open-drain (depending on the technology) outputs.

Brief Summary Text (9):
The I2C bus (and similar arrangements) interface is constructed around an input buffer and an open-drain or open-collector transistor. When nothing is happening on the bus, the bus lines are in a logic HIGH state or Asserted state. To put information on the bus, a semiconductor device drives its output transistor, thus pulling the bus to a LOW or negated level. Typically an external PULL UP resistor is then utilized to pull the bus lines back to a logic HIGH state when released by the semiconductor device. When the bus is IDLE (no activity) both lines are at a logic HIGH state. These pull up resistors in the devices are often actually small current sources or may even be nonexistent.

Brief Summary Text (11):
However, the open collector technique has a drawback too. If you have a long bus, it will have a serious effect on the speed of the circuit. Long lines present a capacitive load on the output. Since the pull up resistor is passive, the circuit response time (RC time constant) will be reflected onto the shapes of the signals. The higher the RC time constant for a circuit, the slower the response for the

circuit. This is due to the effect that it influences the "sharpness" of the edges of the shapes of the signals for the I2C bus. At a certain point, the logic circuits of a semiconductor die will not be able to distinguish clearly between a logic state 1 and a logic state 0.

Detailed Description Text (4):
FIG. 1 is a block diagram illustrating a two-wire serial bus 60 (hereinafter referred to as "TWS bus 60") coupling a plurality of devices, in accordance with an embodiment of the present invention. In this figure, the TWS bus 60 couples a computer 70, a scanner 72, a CD recorder 73, a monitor 74, a keyboard 75, and a printer 76. This is illustrative only. In one embodiment of the present invention, the TWS bus 60 comprises a Titan bus sold by the Hewlett-Packard Company, Palo Alto, Calif., that utilizes the I2C bus protocol, but varies slightly from such bus in its electrical specifications. Other serial buses are also within the scope of this invention.

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L1: Entry 56 of 201 File: USPT Jul 22, 2003

DOCUMENT-IDENTIFIER: US 6597197 B1
** See image for Certificate of Correction **
TITLE: I2C repeater with voltage translation

Abstract Text (1):
A bus repeater with voltage conversion and multiplexing circuits for use between devices with incompatible voltage levels communicating over inter-integrated circuit (I2C) buses. Bi-directional data and clock lines are passed through the circuit from one bus to the other, blocked so they are not passed on, or modified before being passed on, depending on the current transaction. The repeater is placed between two separate I2C buses and communicates between the two buses. Separating the two buses in this manner permits each bus to operate at a different voltage. Multiplexing is achieved by including logic in the repeater to recognize a first address associated with the repeater received from the first bus, and pass subsequent addresses and their associated messages through to the second bus to be decoded and processed by the devices on that bus. When the first address is not associated with the repeater, subsequent addresses and their associated messages are ignored and not passed through. To accommodate the slow-slave requirements of an I2C bus, the duration of signals on the clock line may be modified.

Brief Summary Text (7):
Bus 18 is typically an inter-integrated circuit bus, frequently referred to as an I.sup.2 C or I2C bus. This is a well-known two-line serial bus with a bi-directional serial data line and a bi-directional clock line. I2C protocol follows a master-slave format, with the master device initiating a transaction and specifying the address of the designated slave device, and the designated slave device responding to it. I2C protocol is fairly simple, with a five-part format: 1) A start bit to initiate a transaction, 2) an address byte, with seven bits denoting the address and the eighth bit denoting a read or write command, 3) data bytes, 4) an acknowledge bit following each 8-bit address or data byte, and 5) a stop bit to terminate the transaction. During the transmission of address and data bits, the data line may change only while the clock line is low. If the data line changes while the clock line is high, this signifies one of two commands: 1) a falling data signal from the master is a START command, and 2) a rising data signal from the master is a STOP command. An ACKNOWLEDGE response from the slave is indicated during an acknowledge bit when the slave pulls the data line low while the clock line is low, and keeps the data line low while the clock line is high. Failure of the slave to pull the data line low during the acknowledge bit is a non-acknowledgment condition and the master will abort the transfer with a stop bit. I2C protocol also allows a slow slave device to make the clock line wait for it. When a responding slave device sees the clock line pulled low, it can also drive the clock line low until it is ready to receive the next clock pulse. This period will normally be less than the period in which the master is driving the clock low (i.e., 4.7 microseconds minimum), and will therefore have no effect. But in the event the slave keeps the line low for longer than this period, the clock line will remain low even after the master device ceases driving it low. When this happens, the master device recognizes this condition as a delay by a slow slave, and delays the start of the next clock cycle until the slave releases the clock line, allowing it to go high.

Brief Summary Text (8):
Memory components such as SDRAMs 16 are typically designed to interface the I2C bus with 3.3 volt logic. However, many system devices now incorporate logic circuits using 1.8 volt logic levels, and can suffer damage if exposed to voltages in excess of about 2.2 volts. Thus, connecting these 1.8 volt system devices directly to a standard 3.3 volt SDRAM through an I2C bus can result in damage to the system device's interface circuitry.

Detailed Description Text (2):
FIG. 2 shows a system 2 of the present invention. System component 10 initiates communications with multiple memory data components (MDC) 12 over bus 14. System component 10 may have various forms. For instance, it might be an integrated circuit dedicated to the functions described herein, or it might be a processor which also performs many other functions. Each MDC 12 can communicate over its respective bus 18 with any device 16 connected to that bus, such as synchronous dynamic random access memories (SDRAM). In one embodiment, bus 18 and SDRAMs 16 can be the same devices shown in the prior art of FIG. 1. The voltage used on bus 14 should be chosen for compatibility with system component 10, such as 1.8 volts. The voltage used on bus 18 should be chosen for compatibility with memory components 16, such as 3.3 volts. FIG. 2 shows four NDCs 12, with eight SDRAMs 16 per MDC, although other quantities can also be used. Buses 14 and 18 can both be I2C buses. In one embodiment, each MDC 12 can perform several functions, including 1) voltage translation between bus 14 and bus 18, 2) multiplexing of address data between bus 14 and bus 18, and 3) manipulation of the clock line between bus 14 and bus 18 to accommodate slow slave devices. Each MDC can function as a repeater by receiving logic signals on one bus and duplicating those logic signals on the other bus, even if each bus operates at a different voltage level. Each MDC has a data circuit 30 for processing the data signals, a clock circuit 60 for processing the clock signals, and a control circuit 90 for providing overall control of the MDC. In the embodiment shown in FIG. 2, each MDC is identical except for its bus address on bus 14.

Detailed Description Text (3):
FIG. 3 shows a circuit 30 for processing data signals SDA for an I2C bus, while FIG. 5 shows a circuit 60 for processing clock signals SCL for an I2C bus. Bus 14 contains a bidirectional data line 13 and a bidirectional clock line 17. Bus 18 contains a bidirectional data line 15 and a bidirectional clock line 19.

Detailed Description Text (13):
In a preferred embodiment, clock control circuit 70 includes a state machine. FIG. 6 shows a state diagram of its operation. The action labels in FIG. 6 show logic conditions rather than voltages, and follow the inverse logic convention previously described (i.e., `Drive3.3V=1` means line 19 to the 3.3 volt slave device is driven low, which is a logic 1). The state machine initially loops at step 600 in an idle condition. When an input from a master device (shown as SCL1.8V from system component 10) goes low, the state machine goes to step 610 by driving both line 17 and line 19 low. This has no effect on line 17, which is already low, but initiates a low signal to the slave device on line 19, thus passing the low clock signal from master to slave. Following the I2C protocol, the affected slave device can, if so configured, respond to this by also driving line 19 low until it is ready to receive the next clock signal. At this point, the operation of the state machine is not affected by the slave's response, so the state diagram does not indicate this condition. At step 610, a time-out counter is loaded and the state machine advances to step 620, where it waits for the counter to time out. The counter should be set to time out in no more than the period of time the clock line will be held low by the master, which is a minimum of 4.7 microseconds under the I2C standards. In one embodiment, the I2C bus clock runs at 100 KHz with a 50% duty cycle, holding the clock line low for 5 microseconds. When the counter times out, the state machine advances to step 630 by releasing line 19 to the slave, allowing line 19 to go high (logic 0). What happens at step 630 depends on what the slave device is doing. If

the slave device has completed its internal processing and released the line (stopped driving it low), then line 19 will be high and the state machine will release line 17 to the master. In most cases, the master will continue to hold line 17 low another 0.3 micro-seconds until it completes the 5 micro-second low period of the clock signal (assuming the above 100 KHz clock). The state machine then advances to step 600 to restart the process. However, if the slave device has not completed its internal processing, it indicates a slow-slave condition by continuing to hold line 19 low. In this case, the state machine will continue to hold line 17 low to the master until the slave releases line 19. When the master device releases clock line 17 but sees it is still being held low, the master recognizes this as the slow-slave condition, and delays further clocked operations until it sees clock line 17 go high, indicating the slave has completed its processing. In this manner, the state machine can pass a normal clock signal from master to slave, and can also pass a slow-slave signal from slave to master.

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L8: Entry 300 of 305 File: USPT Aug 8, 1978

DOCUMENT-IDENTIFIER: US 4106091 A
TITLE: Interrupt status indication logic for polled interrupt digital system

Detailed Description Text (24):
Referring to FIG. 4, digital system 170 includes a microprocessor chip 172, an interface adaptor circuit which advantageously is an asynchronous communications interface adaptor chip 10 as described above, and two additional interface adaptors 10' and 10" all coupled to bidirectional data bus 14. ACIA chip 10 is coupled to a peripheral device 210, which could be a modem, by transmitter data conductor 108, receiver data conductor 122, and DCD conductor 92. IRQ interrupt output conductor 118 is connected to a common interrupt conductor 118' connected to microprocessor unit 172 and to interrupt output conductors of interface adaptors 10, 10', and 10" each of which is normally coupled to other peripheral devices (not shown). ACIA chip 10 includes interrupt logic 50 which includes a combination of logic gates 182, 186, 194, and 196. The inputs to this combinational logic gate are conductors 188, 190 and 192, which are outputs of interrupt source circuits 178, 176, and 174, respectively. The other inputs to the combinational logic gate are interrupt enable inputs coupled to control circuitry in FIG. 1. The combinational logical gate is essentially an OR type gate which provides a signal at its output indicating whether any of the interrupt sources 178, 176, or 174 are in an "active" state, that is whether any of them are indicating an interrupt condition, and whether their respective interrupt enable is in an "active" condition. If so, an interrupt signal is sent out via IRQ conductor 118 and is detected by microprocessor 172. The interrupt indication signal also is conducted by conductor 200 to an input of gate 202, which is bit 7 of the status register 34, and (upon application of a proper read status signal at node 204, which is coupled to the other input of gate 202) is transferred to the bidirectional data bus in a preferred embodiment of the invention. If the microprocessor 172 fetches a status word, the state of conductor 200 in interrupt logic circuit 750 may be communicated via buffer circuit 208 of buffer section 12 to data bus 14 and thus to microprocessor 172 for further data processing operations thereon.

L1: Entry 4 of 5 File: USPT May 20, 1997

DOCUMENT-IDENTIFIER: US 5631850 A
TITLE: Audio visual equipment with a digital bus system and method for initializing and confirming connection

Detailed Description Text (36):
The D2B protocol communications processing microcomputer 109 having RAMS and ROMS and the like internally constructed for its own exclusive use (hereinafter referred to as the D2B communications processing microcomputer) is connected to the picture display IC 114 and the switcher 118 via the internal bus 120 derived from the I2C bus (i.e. the so called Domestic Digital Bus). It is also serially connected for the sending and receiving of commands to other equipment such as the first VCR 30, the second VCR 40 and the laser disc player 50 via the D2B communications processing IC 110 and the D2B control line 121.

Detailed Description Text (122):
FIG. 27 is a block diagram showing the internal process structure for the D2B microcomputer 109 in FIG. 3, FIG. 28 is a block diagram showing the breakdown of the D2B module and FIG. 29 is a flowchart showing the process for the D2B microcomputer 109. In FIG. 29, when the power is turned on (step S371), the microcomputer 109 initializes the CPU (step S372). The D2BWORK, which is a register in which initialization set up information related to the D2B processes is stored, is then initialized (step S373) and peripheral ICs such as the picture display IC 114 and the D2B communications processing IC 110 are also initialized (step S374). The bus protocol process for the I2C bus belonging to the internal bus is then initialized (step S375)and the address initialization is then carried out (step S376). This then completes the initialization of the D2B microcomputer 109.

US-PAT-NO: 4855730

DOCUMENT-IDENTIFIER: US 4855730 A

TITLE: Component audio/video system with timed control of plural peripheral devices

---------- KWIC ---------

US Patent No. - PN (1):
4855730

Detailed Description Text - DETX (5):
In operation of the portion of the system described thus far, the user sends device selection and operating mode control command information to system controller 60 by depressing keys on remote control unit 68 which, in turn, transmits the commands to a selected peripheral audio/video device (12-24). The "slave" or remote control processors 80-92 acknowledge receipt of messages from the "master" system controller by transmitting a status message back to the master system controller 60 via the bi-directional data bus 32. R. A. Pitsch in the aforementioned article describes a suitable bus communication protocol. The status information returned via bus 32 may be displayed on the screen of TV receiver 10 for informing the user of the current operating modes of the selected peripheral device.

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L2: Entry 1 of 1 File: USPT Nov 25, 2003

US-PAT-NO: 6653863
DOCUMENT-IDENTIFIER: US 6653863 B1

TITLE: Method and apparatus for improving bus capacity

DATE-ISSUED: November 25, 2003

INVENTOR-INFORMATION:

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APPL-NO: 10/ 108082 [PALM]
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INT-CL: [07] H03 K 19/075

US-CL-ISSUED: 326/82; 326/90, 326/26
US-CL-CURRENT: 326/82; 326/26, 326/90

FIELD-OF-SEARCH: 326/26, 326/82, 326/83, 326/86, 326/89, 326/90

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5905389	May 1999	Alleven	327/108
☐	6356140	March 2002	Bell	327/540
☐	6525609	February 2003	Behzad	330/254

ART-UNIT: 2819

PRIMARY-EXAMINER: Le; Don

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ABSTRACT:

A two-wire serial bus allows bus mastering by any device on the bus utilizing bus pull-ups. In systems with long bus lengths or large numbers of devices, rise times suffer unless accelerated. An operational amplifier (Op Amp) controlled current source is utilized to provide pull-up current for bus lines. The Op Amp provides precise control of the current value and the slew rate required to meet stringent demands of the two-wire serial bus. A voltage divider sets the input voltage to the Op Amp, and a transistor gates the Op Amp current to the bus until it saturates.

24 Claims, 4 Drawing figures

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